09-08-00

A

Practitioner's Docket No. 198-0191

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Box Patent Application
Assistant Commissioner for Patents
Washington, D.C. 20231

NEW APPLICATION TRANSMITTAL

Transmitted herewith for filing is the patent application of
Inventor(s): Jay D. Baker, Myron Lemecha, Delin Li

WARNING: *37 C.F.R. § 1.41(a)(1) points out:*

"(a) A patent is applied for in the name or names of the actual inventor or inventors.

(1) The inventorship of a nonprovisional application is that inventorship set forth in the oath or declaration as prescribed by § 1.63, except as provided for in § 1.53(d)(4) and § 1.63(d). If an oath or declaration as prescribed by § 1.63 is not filed during the pendency of a nonprovisional application, the inventorship is that inventorship set forth in the application papers filed pursuant to § 1.53(b), unless a petition under this paragraph accompanied by the fee set forth in § 1.17(i) is filed supplying or changing the name or names of the inventor or inventors."

For (title): ELECTRICAL CIRCUIT BOARD AND METHOD FOR MAKING THE SAME

CERTIFICATION UNDER 37 C.F.R. 1.10*
*(Express Mail label number is **mandatory**.)*
(Express Mail certification is optional.)

I hereby certify that this correspondence and the documents referred to as attached therein are being deposited with the United States Postal Service on this date 09/06/2000, in an envelope as "Express Mail Post Office to Addressee," mailing Label Number _____, addressed to the: Assistant Commissioner for Patents, Washington, D.C. 20231.

EK902334730US

Tami C Williams
(type or print name of person mailing paper)

Tami C Williams
Signature of person mailing paper

WARNING: *Certificate of mailing (first class) or facsimile transmission procedures of 37 C.F.R. 1.8 cannot be used to obtain a date of mailing or transmission for this correspondence.*

***WARNING:** Each paper or fee filed by "Express Mail" **must** have the number of the "Express Mail" mailing label placed thereon prior to mailing. 37 C.F.R. 1.10(b).*
*"Since the filing of correspondence under § 1.10 without the Express Mail mailing label thereon is an oversight that can be avoided by the exercise of reasonable care, requests for waiver of this requirement will **not** be granted on petition." Notice of Oct. 24, 1996, 60 Fed. Reg. 56,439, at 56,442.*

1. Type of Application

This new application is for a(n)

(check one applicable item below)

[x] Original (nonprovisional)
[ ] Design
[ ] Plant

WARNING: ***Do not*** *use this transmittal for a completion in the U.S. of an International Application under 35 U.S.C. 371(c)(4), unless the International Application is being filed as a divisional, continuation or continuation-in-part application.*

WARNING: ***Do not*** *use this transmittal for the filing of a provisional application.*

NOTE: If one of the following 3 items apply, then complete and attach ADDED PAGES FOR NEW APPLICATION TRANSMITTAL WHERE BENEFIT OF A PRIOR U.S. APPLICATION CLAIMED and a NOTIFICATION IN PARENT APPLICATION OF THE FILING OF THIS CONTINUATION APPLICATION.

[ ] Divisional.
[ ] Continuation.
[ ] Continuation-in-part (C-I-P).

2. Benefit of Prior U.S. Application(s) (35 U.S.C. 119(e), 120, or 121)

NOTE: A nonprovisional application may claim an invention disclosed in one or more prior filed copending nonprovisional applications or copending international applications designating the United States of America. In order for a nonprovisional application to claim the benefit of a prior filed copending nonprovisional application or copending international application designating the United States of America, each prior application must name as an inventor at least one inventor named in the later filed nonprovisional application and disclose the named inventor's invention claimed in at least one claim of the later filed nonprovisional application in the manner provided by the first paragraph of 35 U.S.C. 112. Each prior application must also be:

(i) An international application entitled to a filing date in accordance with PCT Article 11 and designating the United States of America; or

(ii) Complete as set forth in § 1.51(b); or

(iii) Entitled to a filing date as set forth in § 1.53(b) or § 1.53(d) and include the basic filing fee set forth in § 1.16; or

(iv) Entitled to a filing date as set forth in § 1.53(b) and have paid therein the processing and retention fee set forth in § 1.21(l) within the time period set forth in § 1.53(f).

37 C.F.R. § 1.78(a)(1).

NOTE If the new application being transmitted is a divisional, continuation or a continuation-in-part of a parent case, or where the parent case is an International Application which designated the U.S., or benefit of a prior provisional application is claimed, then check the following item and complete and attach ADDED PAGES FOR NEW APPLICATION TRANSMITTAL WHERE BENEFIT OF PRIOR U.S. APPLICATION(S) CLAIMED.

WARNING: *If an application claims the benefit of the filing date of an earlier filed application under 35 U.S.C. 120, 121*

or 365(c), the 20-year term of that application will be based upon the filing date of the earliest U.S. application that the application makes reference to under 35 U.S.C. 120, 121 or 365(c). (35 U.S.C. 154(a)(2) does not take into account, for the determination of the patent term, any application on which priority is claimed under 35 U.S.C. 119, 365(a) or 365(b).) For a c-i-p application, applicant should review whether any claim in the patent that will issue is supported by an earlier application and, if not, the applicant should consider canceling the reference to the earlier filed application. The term of a patent is not based on a claim-by-claim approach. See Notice of April 14, 1995, 60 Fed. Reg. 20,195, at 20,205.

WARNING: *When the last day of pendency of a provisional application falls on a Saturday, Sunday, or Federal holiday within the District of Columbia, any nonprovisional application claiming benefit of the provisional application* ***must*** *be filed prior to the Saturday, Sunday, or Federal holiday within the District of Columbia. See 37 C.F.R. § 1.78(a)(3).*

[ ] The new application being transmitted claims the benefit of prior U.S. application(s). Enclosed are ADDED PAGES FOR NEW APPLICATION TRANSMITTAL WHERE BENEFIT OF PRIOR U.S. APPLICATION(S) CLAIMED.

3. Papers Enclosed

A. Required for Filing Date under 37 C.F.R. § 1.53(b) (Regular) or 37 C.F.R. § 1.153 (Design) Application

_17__ Pages of Specification
__5__ Pages of Claims
__5__ Sheets of Drawing

WARNING: ***DO NOT*** *submit original drawings. A high quality copy of the drawings should be supplied when filing a patent application. The drawings that are submitted to the Office must be on strong, white, smooth, and non-shiny paper and meet the standards according to § 1.84. If corrections to the drawings are necessary, they should be made to the original drawing and a high-quality copy of the corrected original drawing then submitted to the Office. Only one copy is required or desired. For comments on proposed then-new 37 C.F.R. 1.84, see Notice of March 9, 1988 . (1990 O.G. 57-62).*

NOTE: "Identifying indicia, if provided, should include the application number or the title of the invention, inventor's name, docket number (if any), and the name and telephone number of a person to call if the Office is unable to match the drawings to the proper application. This information should be placed on the back of each sheet of drawing a minimum distance of 1.5 cm. (5/8 inch) down from the top of the page. . . " 37 C.F.R. § 1.84(c)).

(complete the following, if applicable)

[ ] The enclosed drawing(s) are photograph(s), and there is also attached a "PETITION TO ACCEPT PHOTOGRAPH(S) AS DRAWING(S)." 37 C.F.R. § 1.84(b).

[x] Formal
[ ] Informal

B. Other Papers Enclosed

___ Pages of declaration and power of attorney
___1_ Pages of Abstract
____ Other

4. Additional Papers Enclosed

[ ] Amendment to claims

[ ] Cancel in this applications claims _____ before calculating the filing fee. (At least one original independent claim must be retained for filing purposes.)

[ ] Add the claims shown on the attached amendment. (Claims added have been numbered consecutively following the highest numbered original claims.)

[ ] Preliminary Amendment
[ ] Information Disclosure Statement (37 C.F.R. § 1.98)
[ ] Form PTO-1449 (PTO/SB/08A and 08B)
[ ] Citations
[ ] Declaration of Biological Deposit
[ ] Submission of "Sequence Listing," computer readable copy and/or amendment pertaining thereto for biotechnology invention containing nucleotide and/or amino acid sequence.
[ ] Authorization of Attorney(s) to Accept and Follow Instructions from Representative
[ ] Special Comments
[ ] Other

5. Declaration or Oath (including power of attorney)

NOTE: A newly executed declaration is not required in a continuation or divisional application provided the prior nonprovisional application contained a declaration as required, the application being filed is by all or fewer than all the inventors named in the prior application, there is no new matter in the application being filed, and a copy of the executed declaration filed in the prior application (showing the signature or an indication thereon that it was signed) is submitted. The copy must be accompanied by a statement requesting deletion of the names of person(s) who are not inventors of the application being filed. If the declaration in the prior application was filed under § 1.47 then a copy of that declaration must be filed accompanied by a copy of the decision granting § 1.47 status or, if a nonsigning person under § 1.47 has subsequently joined in a prior application, then a copy of the subsequently executed declaration must be filed. See 37 C.F.R. § 1.63(d)(1)-(3).

NOTE: A declaration filed to complete an application must be executed, identify the specification to which it is directed, identify each inventor by full name, including the family name, and at least one given name without abbreviation together with any other given name or initial, and the residence, post office address and country of citizenship of each inventor, and state whether the inventor is a sole or joint inventor. 37 C.F.R. § 1.63(a)(1)-(4).

[ ] Enclosed

Executed by

(check **all** *applicable boxes)*

[ ] inventor(s).
[ ] legal representative of inventor(s). 37 C.F.R. § 1.42 or 1.43.
[ ] joint inventor or person showing a proprietary interest on behalf of inventor who refused to sign or cannot be reached.

[ ] This is the petition required by 37 C.F.R. § 1.47 and the statement

required by 37 C.F.R. § 1.47 is also attached. See item 13 below for fee.

[x] Not Enclosed.

NOTE: Where the filing is a completion in the U.S. of an International Application, or where the completion of the U.S. application contains subject matter in addition to the International Application, the application may be treated as a continuation or continuation-in-part, as the case may be, utilizing ADDED PAGE FOR NEW APPLICATION TRANSMITTAL WHERE BENEFIT OF PRIOR U.S. APPLICATION CLAIMED.

[ ] Application is made by a person authorized under 37 C.F.R. 1.41(c) on behalf of *all* the above named inventor(s).

(The declaration or oath, along with the surcharge required by 37 C.F.R. § 1.16(e), can be filed subsequently).

[ ] Showing that the filing is authorized.
(not required unless called into question. 37 C.F.R. § 1.41(d))

6. Inventorship Statement

WARNING: If the named inventors are each not the inventors of all the claims an explanation, including the ownership of the various claims at the time the last claimed invention was made, should be submitted.

The inventorship for all the claims in this application are:

[x] The same.

or

[ ] Not the same. An explanation, including the ownership of the various claims at the time the last claimed invention was made,
[ ] is submitted.
[ ] will be submitted.

7. Language

NOTE: An application including a signed oath or declaration may be filed in a language other than English. An English translation of the non-English language application and the processing fee of $130.00 required by 37 C.F.R. § 1.17(k) is required to be filed with the application, or within such time as may be set by the Office. 37 C.F.R. § 1.52(d).

[x] English
[ ] Non-English

[ ] The attached translation includes a statement that the translation is accurate. 37 C.F.R. § 1.52(d).

8. Assignment

[ ] An assignment of the invention to _____

_____

[ ] is attached. A separate [ ] "COVER SHEET FOR ASSIGNMENT (DOCUMENT) ACCOMPANYING NEW PATENT APPLICATION" or [ ] FORM PTO 1595 is also attached.

[x] will follow.

NOTE: "If an assignment is submitted with a new application, send two separate letters-one for the application and one for the assignment" Notice of May 4, 1990 (1114 O.G. 77-78).

WARNING: *A newly executed "STATEMENT UNDER 37 C.F.R. § 3.73(b)" must be filed when a continuation-in-part application is filed by an assignee. Notice of April 30, 1993, 1150 O.G. 62-64.*

9. Certified Copy

Certified copy(ies) of application(s)

Country	Appln. no.	Filed
Country	Appln. no.	Filed
Country	Appln. no.	Filed

from which priority is claimed

[ ] is (are) attached.

[ ] will follow.

NOTE: The foreign application forming the basis for the claim for priority must be referred to in the oath or declaration. 37 C.F.R. § 1.55(a) and 1.63.

NOTE: This item is for any foreign priority for which the application being filed directly relates. If any parent U.S. application or International Application from which this application claims benefit under 35 U.S.C. 120 is itself entitled to priority from a prior foreign application, then complete item 18 on the ADDED PAGES FOR NEW APPLICATION TRANSMITTAL WHERE BENEFIT OF PRIOR U.S. APPLICATION(S) CLAIMED.

10. Fee Calculation (37 C.F.R. § 1.16)

A. [x] Regular application

CLAIMS AS FILED

Claims	Number Filed	Basic Fee Allowance	Number Extra	Rate	Basic Fee 37 C.F.R. § 1.16(a) $760.00
Total Claims (37 C.F.R. § 1.16(c))	20	~~- 20 =~~	x	~~$ 18.00~~	
Independent Claims (37 C.F.R. § 1.16(b))	3	- 3 =	x	$ 78.00	
Multiple Dependent Claim(s), if any (37 C.F.R. § 1.16(d))			+	$260.00	

[ ] Amendment cancelling extra claims is enclosed.
[ ] Amendment deleting multiple-dependencies is enclosed.
[ ] Fee for extra claims is not being paid at this time.

NOTE: If the fees for extra claims are not paid on filing they must be paid or the claims cancelled by amendment, prior to the expiration of the time period set for response by the Patent and Trademark Office in any notice of fee deficiency. 37 C.F.R. § 1.16(d).

Filing Fee Calculation $ 690.00

B. [ ] Design application
($310.00—37 C.F.R. § 1.16(f))
Filing Fee Calculation $_____

C. [ ] Plant application
($480.00—37 C.F.R. § 1.16(g))
Filing Fee Calculation $_____

11. Small Entity Statement(s)

[ ] Statement(s) that this is a filing by a small entity under 37 C.F.R. §§ 1.9 and 1.27 is (are) attached.

WARNING: *"Status as a small entity must be specifically established in each application or patent in which the status is available and desired. Status as a small entity in one application or patent does not affect any other application or patent, including applications or patents which are directly or indirectly dependent upon the application or patent in which the status has been established. The refiling of an application under § 1.53 as a continuation, division, or continuation-in-part (including a continued prosecution application under § 1.53(d)), or the filing of a reissue application requires a new determination as to continued entitlement to small entity status for the continuing or reissue application. A nonprovisional application claiming benefit under 35 U.S.C. 119(e), 120, 121, or 365(c) of a prior application, or a reissue application may rely on a statement filed in the prior application or in the patent if the nonprovisional application or the reissue application includes a reference to the statement in the prior application or in the patent or includes a copy of the statement in the prior application or in the patent and status as a small entity is still proper and desired. The payment of the small entity basic statutory filing fee will be treated as such a reference for purposes of this section." 37 C.F.R. § 1.28(a)(2).*

(complete the following, if applicable)

[ ] Status as a small entity was claimed in prior application _____/_____, filed on _____ from which benefit is being claimed for this application under:

35 U.S.C. § [ ] 119(e),
[ ] 120,
[ ] 121,
[ ] 365(c),

and which status as a small entity is still proper and desired.

[ ] A copy of the statement in the prior application is included.

Filing Fee Calculation (50% of **A**, **B** or **C** above) $_____

NOTE: Any excess of the full fee paid will be refunded if a small entity status is established refund request are filed within 2 months of the date of timely payment of a full fee. The two-month period is not extendable under § 1.136. 37 C.F.R. § 1.28(a).

12. Request for International-Type Search (37 C.F.R. § 1.104(d))

(complete, if applicable)

[ ] Please prepare an international-type search report for this application at the time when national examination on the merits takes place.

13. Fee Payment Being Made at This Time

[ ] Not Enclosed

[ ] No filing fee is to be paid at this time.
(This and the surcharge required by 37 C.F.R. § 1.16(e) can be paid subsequently.)

[x] Enclosed

[ ] Filing fee $ 690.00

[ ] Recording assignment
($40.00; 37 C.F.R. § 1.21(h))
(See attached "COVER SHEET FOR ASSIGNMENT ACCOMPANYING NEW APPLICATION.") $_____

[ ] Petition fee for filing by other than all the inventors or person on behalf of the inventor where inventor refused to sign or cannot be reached
($130.00; 37 C.F.R. §§ 1.47 and 1.17(i)) $_____

[ ] For processing an application with a specification in a non-English language
($130.00; 37 C.F.R. §§ 1.52(d) and 1.17(k)) $_____

[ ] Processing and retention fee
($130.00; 37 C.F.R. §§ 1.53(d) and 1.21(l)) $_____

[ ] Fee for international-type search report
($40.00; 37 C.F.R. § 1.21(e)) $_____

NOTE: 37 C.F.R. § 1.21(l) establishes a fee for processing and retaining any application that is abandoned for failing to complete the application pursuant to 37 C.F.R. § 1.53(f) and this, as well as the changes to 37 C.F.R. § 1.53 and 1.78(a)(1), indicate that in order to obtain the benefit of a prior U.S. application, either the basic filing fee must be paid, or the processing and retention fee of § 1.21(l) must be paid, within 1 year from notification under § 53(f).

Total Fees Enclosed $ 690.00

14. Method of Payment of Fees

[x] Check in the amount of $ 690.00 .

[ ] Charge Account No. _____ in the amount of $_____.
A duplicate of this transmittal is attached.

NOTE: Fees should be itemized in such a manner that it is clear for which purpose the fees are paid. 37 C.F.R. § 1.22(b).

15. Authorization to Charge Additional Fees

WARNING: *If no fees are to be paid on filing, the following items should not be completed.*

WARNING: *Accurately count claims, especially multiple dependent claims, to avoid unexpected high charges, if extra claim charges are authorized.*

[x] The Commissioner is hereby authorized to charge the following additional fees by this paper and during the entire pendency of this application to Account No. 03-1723.

[x] 37 C.F.R. § 1.16(a), (f) or (g) (filing fees)

[x] 37 C.F.R. § 1.16(b), (c) and (d) (presentation of extra claims)

NOTE: Because additional fees for excess or multiple dependent claims not paid on filing or on later presentation must only be paid or these claims cancelled by amendment prior to the expiration of the time period set for response by the PTO in any notice of fee deficiency (37 C.F.R. § 1.16(d)), it might be best not to authorize the PTO to charge additional claim fees, except possibly when dealing with amendments after final action.

[x] 37 C.F.R. § 1.16(e) (surcharge for filing the basic filing fee and/or declaration on a date later than the filing date of the application)

[x] 37 C.F.R. § 1.17(a)(1)-(5) (extension fees pursuant to § 1.136(a).

[x] 37 C.F.R. § 1.17 (application processing fees)

NOTE: "A written request may be submitted in an application that is an authorization to treat any concurrent or future reply, requiring a petition for an extension of time under this paragraph for its timely submission, as incorporating a petition for extension of time for the appropriate length of time. An authorization to charge all required fees, fees under § 1.17, or all required extension of time fees will be treated as a constructive petition for an extension of time in any concurrent or future reply requiring a petition for an extension of time under this paragraph for its timely submission. Submission of the fee set forth in § 1.17(a) will also be treated as a constructive petition for an extension of time in any concurrent reply requiring a petition for an extension of time under this paragraph for its timely submission." 37 C.F.R. § 1.136(a)(3).

[ ] 37 C.F.R. § 1.18 (issue fee at or before mailing of Notice of Allowance, pursuant to 37 C.F.R. § 1.311(b))

NOTE: Where an authorization to charge the issue fee to a deposit account has been filed before the mailing of a Notice of Allowance, the issue fee will be automatically charged to the deposit account at the time of mailing the notice of allowance. 37 C.F.R. § 1.311(b)).

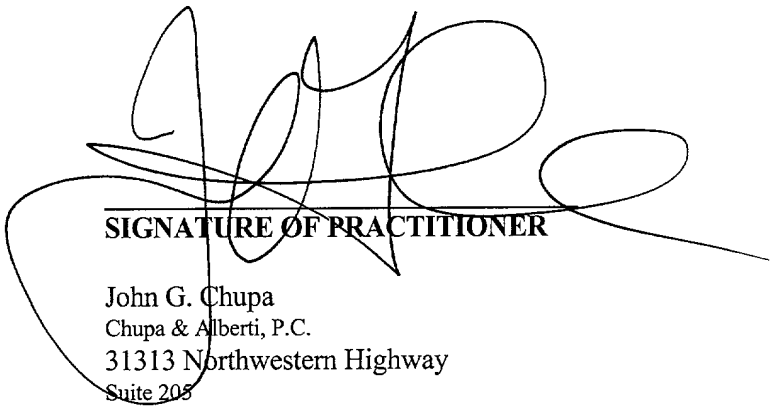
NOTE: 37 C.F.R. § 1.28(b) requires "Notification of any change in status resulting in loss of entitlement to small entity status must be filed in the application . . . prior to paying, or at the time of paying, . . issue fee." From the wording of 37 C.F.R. § 1.28(b), (a) notification of change of status must be made even if the fee is paid as "other than a small entity" and (b) no notification is required if the change is to another small entity.

16. Instructions as to Overpayment

NOTE: ". . . Amounts of twenty-five dollars or less will not be returned unless specifically requested within a reasonable time, nor will the payer be notified of such amounts; amounts over twenty-five dollars may be returned by check or, if requested, by credit to a deposit account." 37 C.F.R. § 1.26(a).

[x] Credit Account No. 03-1723.

[ ] Refund



SIGNATURE OF PRACTITIONER

Reg. No. 33,483

Tel. No.: (248) 865-9588

John G. Chupa
Chupa & Alberti, P.C.
31313 Northwestern Highway
Suite 205
Farmington Hills, MI 48334

[ ] **Incorporation by reference of added pages**

(check the following item if the application in this transmittal claims the benefit of prior U.S. application(s) (including an international application entering the U.S. stage as a continuation, divisional or C-I-P application) and complete and attach the ADDED PAGES FOR NEW APPLICATION TRANSMITTAL WHERE BENEFIT OF PRIOR U.S. APPLICATION(S) CLAIMED)

[ ] Plus Added Pages for New Application Transmittal Where Benefit of Prior U.S. Application(s) Claimed

Number of pages added _____

[ ] Plus Added Pages for Papers Referred to in Item 4 Above

Number of pages added _____

[ ] Plus added pages deleting names of inventor(s) named on prior application(s) who is/are no longer inventor(s) of the subject matter claimed in this application.

Number of pages added _____

[ ] Plus "Assignment Cover Letter Accompanying New Application"

Number of pages added _____

[x] **Statement Where No Further Pages Added**

(if no further pages form a part of this Transmittal, then end this Transmittal with this page and check the following item)

[x] This transmittal ends with this page.

198-0191

ELECTRICAL CIRCUIT BOARD AND A METHOD FOR MAKING THE SAME

(1) Field of the Invention

The present invention relates to a method for making an electrical circuit board and more particularly, to a method for making a multi-layer electrical circuit board having interconnections between portions or layers of the circuit board.

(2) Background of the Invention

Multi-layer circuit boards contain and/or include electrical components which selectively and operatively populate opposed first and second surfaces (i.e., top and bottom surfaces) of each board (or other respective interior portions of each of the boards), thereby desirably allowing each of the electrical circuit boards to contain and/or include a relatively large amount of electrical components which efficiently and densely populate the respective boards.

It is desirable to allow for communication by and between and/or interconnection of the component containing surfaces and/or portions of an electrical circuit board, thereby allowing the contained electrical components on each side of the board (or within certain interior portions of the board) to cooperatively and

selectively interconnect to form one or more desired electrical circuits. This communication and interconnection may require the use of shared electrical ground planes, the transmittal of electrical power and/or control type signals between each of the component containing surfaces and/or the component containing board portions, and/or the selective and physical connection of various contained components.

One common type of interconnection utilized and/or formed within these types of circuit boards is a connection from a conductive layer or member to a ground layer or ground plane. Conventional methods for connecting a conductive layer or member to a ground plane include "wire bonding" and "end soldering". These conventional methods however cannot be used within multi-layer electronic circuit boards, due to the inherent structure of the boards. Moreover, other prior methods for physically and electrically interconnecting conductive layers or portions and ground layers or portions of multi-layer circuit boards are often relatively complicated, costly and time consuming. These prior methods have also resulted in relatively unreliable or defective connections to be formed, thereby causing certain portions of the formed circuit boards to be unusable or to malfunction.

There is therefore a need for a method for producing a multi-layer electrical circuit board which overcomes some or all of the previously delineated drawbacks of prior circuit boards and which provides for relatively uncomplicated and reliable physical and electrical interconnections between conductive layers and ground layers of the circuit board.

SUMMARY OF THE INVENTION

It is a first object of the present invention to provide a method for producing a multi-layer electrical circuit board which overcomes some or all of the previously delineated drawbacks of prior multi-layer electrical circuit board forming methodologies and techniques.

It is a second object of the invention to provide a method for producing a multi-layer electrical circuit board which allows for the selective, efficient, and reliable interconnection between at least one conductive layer to a ground plane or layer.

According to a first aspect of the present invention, a method for forming a connection within a multi-layer circuit board is provided. The multi-layer circuit board includes a first pre-circuit assembly including a conductive core member, a dielectric member which is attached to a top surface of the conductive core

member, an adhesive layer which is coupled to a top surface of the dielectric member, and a second pre-circuit assembly including a second core member and a first and second conductive member which are respectively attached to a top and bottom surface of the second core member. The method includes the steps of: selectively forming at least one hole through the first pre-circuit assembly in a location where a connection to the conductive core is desired to be formed; registering the second pre-circuit assembly with respect to the first pre-circuit, effective to cause a portion of the second conductive member to reside above the at least one hole; attaching the second pre-circuit assembly to the adhesive layer; and selectively inserting a solderable material within the at least one hole, effective to connect the portion of the second conductive member to the conductive core member.

These and other objects, aspects, and advantages of the present invention will become apparent upon reading the following detailed description in combination with the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

Figures 1(a)-(e) are successive sectional side views of a multi-layer circuit board being produced and/or

formed in accordance with the teachings of a first embodiment of the invention.

Figures 2(a)-(e) are successive sectional side views of a multi-layer circuit board being produced and/or formed in accordance with the teachings of a second embodiment of the invention.

Figures 3(a)-(e) are successive sectional side views of a multi-layer circuit board being produced and/or formed in accordance with the teachings of a third embodiment of the invention.

Figures 4(a)-(e) are successive sectional side views of a multi-layer circuit board being produced and/or formed in accordance with the teachings of a fourth embodiment of the invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT OF THE INVENTION

Referring now to Figures 1(a)-(e), there is shown a method for interconnecting layers of a circuit board assembly 10, which is performed in accordance with the teachings of the preferred embodiment of the invention. Circuit board assembly 10 is formed by "building up" or sequentially adding various layers of certain materials to a substrate, pre-circuit assembly or tri-metal film 12. Pre-circuit assembly 12 includes a core metal portion 14, which is preferably manufactured and/or formed from a

conventional aluminum material, and a pair of electrically conductive layers 16, 18 which are respectively attached to the opposing surfaces (e.g., top and bottom surfaces) of core metal portion 12 and which are preferably manufactured and/or formed from a conventional solderable material (e.g. copper). While copper and aluminum are used to form circuit board 10 in the preferred embodiment of the invention, it should be appreciated that other metals and metal combinations can be used to form circuit boards described herein, and may include metals such as iron, nickel, silver, gold, tin and alloys thereof. A dielectric layer 20 is attached/coupled to the top surface of conductive layer 16, and a conventional adhesive layer 22 is applied to and substantially covers the top surface of layer 20. In one non-limiting embodiment, dielectric layer 20 may range from approximately one millimeter to several millimeters in thickness, and adhesive layer 22 may range from approximately 0.5 millimeters to several millimeters in thickness.

As shown in Figure 1(b), a second pre-circuit assembly 24, including a core member 26 which is substantially similar to member 14 and a pair of conductive members or layers 28, 30 which are respectively substantially similar to layers 16, 18, is attached to pre-circuit assembly 12. Particularly, pre-

circuit assembly 24 is attached to pre-circuit assembly 12 by use of an adhesive layer 22 which operatively bonds the conductive layer 30 of pre-circuit assembly 24 to dielectric layer 20. In one non-limiting embodiment of the invention, pre-circuit assembly 24 and/or electrically conductive member 30 is connected, coupled, and/or attached to layer 20 by adhesive 22 by use of a known and conventional laminating process such as a conventional "one-step" laminating process.

After assembly 24 is attached to layer 22, aluminum member 26 is selectively etched away to form the circuit board illustrated in Figure 1(c). Next, portions of portions of dielectric layer 20, adhesive layer 22 and conductive layer 30 are locally, mechanically and/or chemically removed from areas of circuit board 10 where connections between conductor 30 and substrate metal 16 are desired to be formed, thereby forming holes, cavities or vias 34 illustrated in Figure 1(d). In the preferred embodiment of the invention, a conventional drilling device and/or procedure is used to selectively remove areas of layers 20, 22. In alternate embodiments, other conventional removal processes are utilized.

Finally, as illustrated in Figure 1(e), amounts of a solder or conductive material 36 are selectively inserted into the formed vias 34 after the portions of layers 30, 22 and 20 have been selectively removed. The solder or

conductive material 36 is effective to provide a robust and reliable connection between layers 30 and 16. In the preferred embodiment of the invention, solder material 36 is selectively inserted or deposited into vias 34 in a molten state. In alternative embodiments, solder material 36 is selectively inserted or deposed into vias 34 by use of a conventional compression printing technique. In other alternate embodiments, solder material 36 may be selectively inserted into vias 34 by use of a laser solder, reflow, wave solder or other conventional soldering method.

Referring now to Figures 2(a)-(e), there is shown a method for interconnecting layers of a circuit assembly 50, which is performed in accordance with the teachings of a second embodiment of the invention. Circuit assembly 50 is formed by "building up" or sequentially adding various layers of certain materials to a "substrate" portion 52. Substrate portion 52 includes a core metal portion or ground layer 54, which is preferably manufactured and/or formed from a conventional solderable material (e.g. copper). A dielectric layer 56 is attached/coupled to the top surface of conductive layer 54 in a conventional manner, and an conventional adhesive layer 58 is applied to and substantially covers the top surface of layer 56. In one non-limiting embodiment, dielectric layer 58 may comprise conventional

and commercially available "PET", "PEN" or "FR-4" material.

In the first step of the process, as shown in Figure 2(b), through holes or vias 60 are formed through substrate portion 52 in a conventional manner (e.g., by drilling). The through holes 60 are formed in locations where connections between ground member 54 and other portions of the circuit 50 are desired to be formed. After vias 60 are formed, a second pre-circuit assembly 64 is attached to substrate portion 52, as shown in Figure 2(c). Assembly 64 includes a core metal portion 66, which is preferably manufactured and/or formed from a conventional aluminum material, and a pair of electrically conductive layers 68, 70 which are respectively attached to the opposing surfaces (e.g., top and bottom surfaces) of core metal portion 66 and which are preferably manufactured and/or formed from a conventional solderable material (e.g. copper). Pre-circuit assembly 64 is "registered" with respect to holes 60 (e.g., portions of conductive layer 68 which are desired to be connected to ground member 54 are aligned with through holes 60), and is attached to adhesive layer 58 which operatively bonds the conductive layer 68 of pre-circuit assembly 64 to dielectric layer 56. When pre-circuit assembly 64 is attached to dielectric layer 56, portions of conductive layer 68 which are to be

connected to core member 54 extend within or above apertures 60. In one non-limiting embodiment of the invention, pre-circuit assembly 64 and/or electrically conductive member 68 is connected, coupled, and/or attached to adhesive material 58 by use of a known and conventional laminating process such as a conventional "one-step" laminating process.

After pre-circuit assembly 64 is attached to layer 58, portions of aluminum member 66 are selectively and conventionally etched away to form the two-layer circuit board illustrated in Figure 2(d). Finally, as illustrated in Figure 2(e), a solder or conductive material 72 is selectively inserted into the apertures 60. The conductive material 72 is effective to provide a robust and reliable connection between layers 54 and 68 (e.g. between core layer 54 and the portions of layer 68 which are disposed within or above apertures 60). In the preferred embodiment of the invention, solder material 72 is selectively inserted or deposited into vias 60 in a molten state. In alternative embodiments, solder material 72 is selectively inserted or deposited into vias 60 by use of a conventional compression printing technique. In other alternate embodiments, solder material 72 may be selectively inserted into vias 60 by use of a laser solder, reflow, wave solder or other conventional soldering method.

Referring now to Figures 3(a)-(e), there is shown a method for interconnecting layers of a circuit assembly 80, which is performed in accordance with the teachings of the preferred embodiment of the invention. Circuit assembly 80 is formed by "building up" or sequentially adding various layers of certain materials to a "substrate" portion 82, which is substantially identical to substrate portion 52. Particularly, substrate portion 82 includes a ground layer or core metal portion 84, which is preferably manufactured and/or formed from a conventional solderable material (e.g. copper). A dielectric layer 86 is attached/coupled to the top surface of conductive layer 84 in a conventional manner, and an conventional adhesive layer 88 is applied to and substantially covers the top surface of layer 86.

In the first step of the process, as shown in Figure 3(a), through holes or vias 90 are formed through substrate portion 82 in a conventional manner (e.g., by drilling). The through holes 90 are formed in locations where connections between ground member 84 and other portions of the circuit 80 are desired to be formed. After vias 90 are formed, a second pre-circuit assembly 94 is attached to substrate portion 82, as shown in Figure 3(b). Assembly 94 includes a core metal portion 96, which is preferably manufactured and/or formed from a conventional aluminum material, and a pair of

electrically conductive layers 98, 100 which are respectively attached to the opposing surfaces (e.g., top and bottom surfaces) of core metal portion 96 and which are preferably manufactured and/or formed from a conventional solderable material (e.g. copper). Pre-circuit assembly 94 is registered with respect to apertures 90 such that a portion of conducting layer 98 resides above each aperture 90 and such that conducting layer 100 does not reside above either aperture 90 (e.g., portions of conducting layer 98 which are desired to be connected to ground member 84 are aligned with through holes 90). Pre-circuit assembly 94 is then attached to adhesive layer 88 which operatively bonds the conductive layer 98 of pre-circuit assembly 94 to dielectric layer 86. When pre-circuit assembly 94 is attached to dielectric layer 56, portions of conductive layer 98 which are to be connected to core member 84 (e.g. portions 102) are disposed within or above apertures 90. In one non-limiting embodiment of the invention, pre-circuit assembly 94 and/or electrically conductive member 98 is connected, coupled, and/or attached to adhesive material 88 by use of a known and conventional laminating process such as a conventional "one-step" laminating process.

After assembly 94 is attached to layer 88, portions of aluminum member 96 are selectively and conventionally

etched away to form the two-layer circuit board illustrated in Figure 3(c). Particularly, once portions of aluminum member 96 have been etched away, bridge portions 102 of member 98 remain extended across apertures 90. In the next step of the method, a force is imparted on bridge portions 102 in the direction of arrows 104, as illustrated in Figure 3(d). In the preferred embodiment, bridge portions 102 are "punched" downward in the direction of arrows 104 by a conventional punching process and/or tool. Finally, as illustrated in Figure 3(e), amounts of a solder or conductive material 106 are selectively inserted into the apertures 90. The solder material 106 is effective to provide a more robust and reliable connection between layer 84 and layer 98 (e.g., bridges 102). In the preferred embodiment of the invention, solder material 106 is selectively inserted or deposited into vias 90 in a molten state. In alternative embodiments, solder material 106 is selectively inserted or deposed into vias 90 by use of a conventional compression printing technique. In other alternate embodiments, solder material 106 may be selectively inserted into vias 90 by use of a laser solder, reflow, wave solder or other conventional soldering method.

Referring now to Figures 4(a)-(e), there is shown a method for interconnecting layers of a circuit assembly 110, which is performed in accordance with the teachings

of the preferred embodiment of the invention. Circuit assembly 110 is formed by "building up" or sequentially adding various layers of certain materials to a "substrate" portion 112, which is substantially identical to substrate portion 52. Particularly, substrate portion 112 includes a ground layer or core metal portion 114, which is preferably manufactured and/or formed from a conventional solderable material (e.g. copper). A dielectric layer 116 is attached/coupled to the top surface of conductive layer 114 in a conventional manner, and a conventional adhesive layer 118 is applied to and substantially covers the top surface of layer 116.

In the first step of the process, as shown in Figure 4(a), through holes or vias 120 are formed through substrate portion 112 in a conventional manner (e.g., by drilling). The through holes 120 are formed in locations where connections between ground member 114 and other portions of the circuit 110 are desired to be formed. After vias 120 are formed, a second pre-circuit assembly 124 is attached to substrate portion 112, as shown in Figure 4(b). Assembly 124 includes a core metal portion 126, which is preferably manufactured and/or formed from a conventional aluminum material, and a pair of electrically conductive layers 128, 130 which are respectively attached to the opposing surfaces (e.g., top and bottom surfaces) of core metal portion 126 and which

are preferably manufactured and/or formed from a conventional solderable material (e.g. copper). Pre-circuit assembly 124 is registered with respect to holes 120 such that a portion of conducting layer 128 resides above each hole 120 and such that conducting layer 130 does not reside above either hole 120 (e.g., portions of conducting layer 128 which are desired to be connected to ground member 114 are aligned with through holes 120). Pre-circuit assembly 124 is then attached to adhesive layer 118 which operatively bonds the conductive layer 128 of pre-circuit assembly 124 to dielectric layer 116. When pre-circuit assembly 124 is attached to dielectric layer 116, portions of conductive layer 128 which are to be connected to core member 84 (e.g. portions 132) extend within or above apertures 120. In one non-limiting embodiment of the invention, pre-circuit assembly 124 and/or electrically conductive member 128 is connected, coupled, and/or attached to adhesive material 118 by use of a known and conventional laminating process such as a conventional "one-step" laminating process.

After assembly 124 is attached to layer 118, portions of aluminum member 126 are selectively and conventionally etched away to form the two-layer circuit board illustrated in Figure 4(c). Particularly, once portions of aluminum member 126 have been etched away, protrusions, tab members or portions 132 of member 128

remain partially extended across apertures 120. In the next step of the method, a force is imparted upon portions 132 in the direction of arrows 134, as illustrated in Figure 4(d). In the preferred embodiment of the invention, bridge portions 132 are "punched" downward in the direction of arrows 134 by a conventional punching process and/or tool, thereby causing portions 132 to abuttingly engage the side walls of apertures 120. Finally, as illustrated in Figure 4(e), amounts of a solder or conductive material 136 are selectively inserted into the holes 120. The solder material 136 is effective to provide a more robust and reliable connection between layer 114 and layer 128 (e.g., bridges 132). In the preferred embodiment of the invention, solder material 136 is selectively inserted or deposited into vias 120 in a molten state. In alternative embodiments, solder material 136 is selectively inserted or deposed into vias 120 by use of a conventional compression printing technique. In other alternate embodiments, solder material 136 may be selectively inserted into vias 120 by use of a laser solder, reflow, wave solder or other conventional soldering method.

It should be understood that the invention is not limited to the exact embodiment or construction which has been illustrated and described but that various changes

may be made without departing from the spirit and the scope of the invention.

WHAT IS CLAIMED IS:

(1) A multi-layer circuit board comprising:

a first pre-circuit assembly including a first conductive member, and an aperture which is formed through said conductive member;

a second pre-circuit assembly which is attached to said first pre-circuit assembly by use of an adhesive material which is disposed between said first pre-circuit assembly and said second pre-circuit assembly, said second pre-circuit assembly including a second conductive member having a portion extending within said aperture; and

a conductive material which is disposed within said aperture, said conductive material being connected to said first conductive member and said portion of said second conductive member which extends within said aperture, thereby electrically connecting said first conductive member and said second conductive member.

(2) The multi-layer circuit board assembly of claim 1 wherein said aperture includes a side wall and wherein said portion of said second conductive member which extends within said aperture comprises a tab member which abuttingly engages said side wall.

(3) The multi-layer circuit board assembly of claim 1 wherein said portion of said second conductive member

which extends within said aperture comprises a bridge member which traverses said aperture.

(4) The multi-layer circuit board of claim 1 wherein said first pre-circuit assembly further comprises a dielectric layer which is disposed between said first conductive member and said second conductive member.

(5) The multi-layer circuit board of claim 4 wherein said second pre-circuit assembly further comprises a third conductive member and a core member which is disposed between said third conductive member and said second conductive member.

(6) The multi-layer circuit board of claim 5 wherein said second and said third conductive member are made from a copper material and said core member is made from an aluminum material.

(7) The multi-layer circuit board of claim 1 wherein said conductive material comprises solder.

(8) A method for forming a connection within a multi-layer circuit board including a first pre-circuit assembly having a first conductive layer, and a second pre-circuit assembly including a second conductive layer, said method comprising the steps of:

forming an aperture within said first pre-circuit assembly;

aligning said second pre-circuit assembly with said first pre-circuit assembly such that a first portion of said second conductive layer resides above said aperture;

attaching said first pre-circuit assembly to said second pre-circuit assembly; and

inserting conductive material into said aperture effective to connect said first portion of said second conductive layer to said first conductive layer.

(9) The method of claim 8 further comprising the steps of:

selectively removing portions of said second pre-circuit assembly which are disposed above said first portion of said second pre-circuit assembly, thereby exposing said first portion of said second pre-circuit assembly; and

deforming said first portion of said second pre-circuit assembly, effective to cause said first portion of said second pre-circuit assembly to extend within said aperture.

(10) The method of claim 9 wherein said first portion of said second pre-circuit assembly is deformed by use of a punching process.

(11) The method of claim 9 wherein said first portion of said second pre-circuit assembly comprises a bridge portion.

(12) The method of claim 9 wherein said first portion of said second pre-circuit assembly comprises a tab portion.

(13) The method of claim 9 wherein said portions of said second pre-circuit assembly are selectively removed by use of an etching process.

(14) A method for forming a connection within a multi-layer circuit board, said multi-layer circuit board including a first pre-circuit assembly including a conductive core member, a dielectric member which is attached to a top surface of said conductive core member, an adhesive layer which is coupled to a top surface of said dielectric member, and a second pre-circuit assembly including a second core member and a first and second conductive member which are respectively attached to a top and bottom surface of said second core member, said method comprising the steps of:

selectively forming at least one hole through said first pre-circuit assembly in a location where a connection to said conductive core member is desired to be formed;

registering said second pre-circuit assembly with respect to said first pre-circuit, effective to cause a portion of said second conductive member to reside above said at least one hole;

attaching said second pre-circuit assembly to said adhesive layer; and

selectively inserting a conductive material within said at least one hole, effective to connect said portion of said second conductive member to said conductive core member.

(15) The method of claim 14 further comprising the step of:

selectively etching at least a portion of said second core member.

(16) The method of claim 14 wherein said conductive material comprises solder.

(17) The method of claim 14 wherein said solder is selectively inserted into said at least one hole by use of a compression printing technique.

(18) The method of claim 14 wherein said conductive core member is manufactured from a copper material.

(19) The method of claim 17 wherein said first and said second conductive member each comprises a copper member.

(20) The method of claim 19 wherein said second core member comprises an aluminum member.

ABSTRACT OF THE DISCLOSURE

A method for forming connections within a multi-layer electronic circuit board 10 which allows for the selective, efficient, and reliable interconnection between at least one conductive layer and a ground plane or layer.

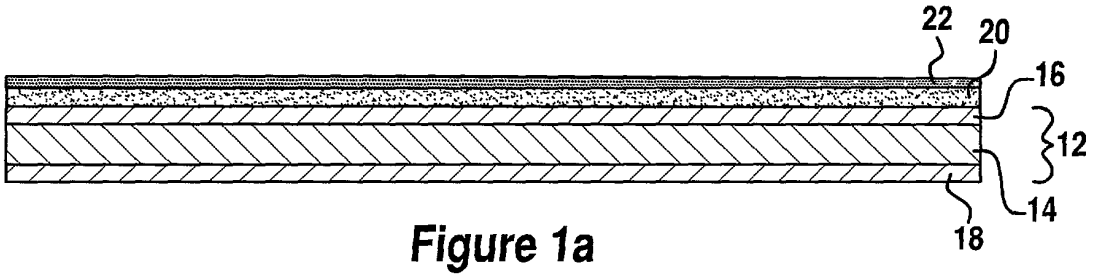


Figure 1a

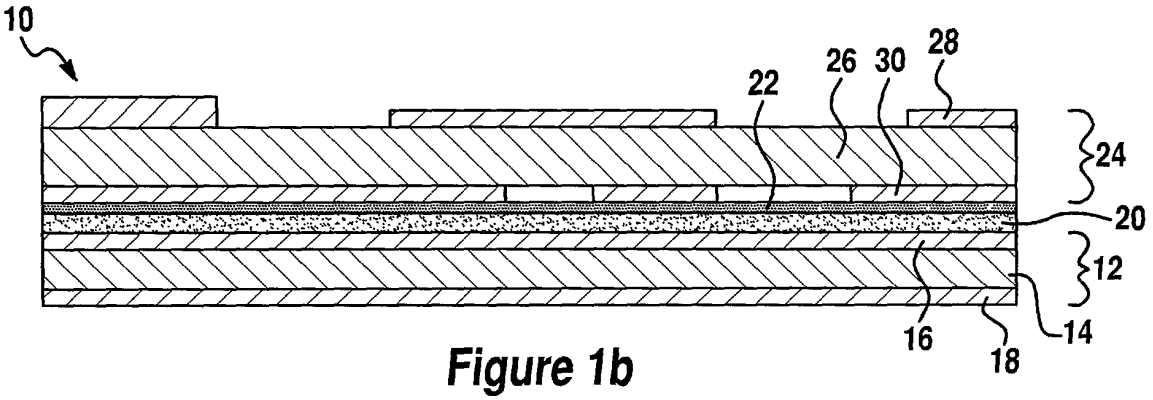


Figure 1b

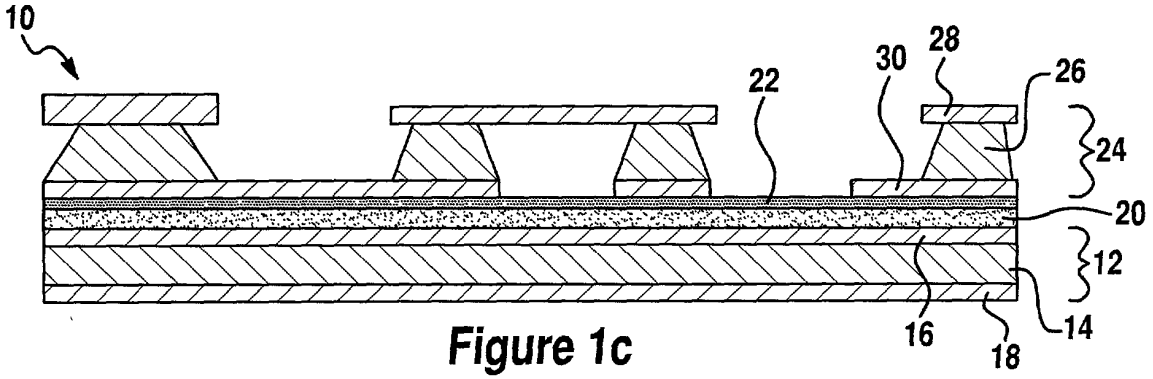


Figure 1c

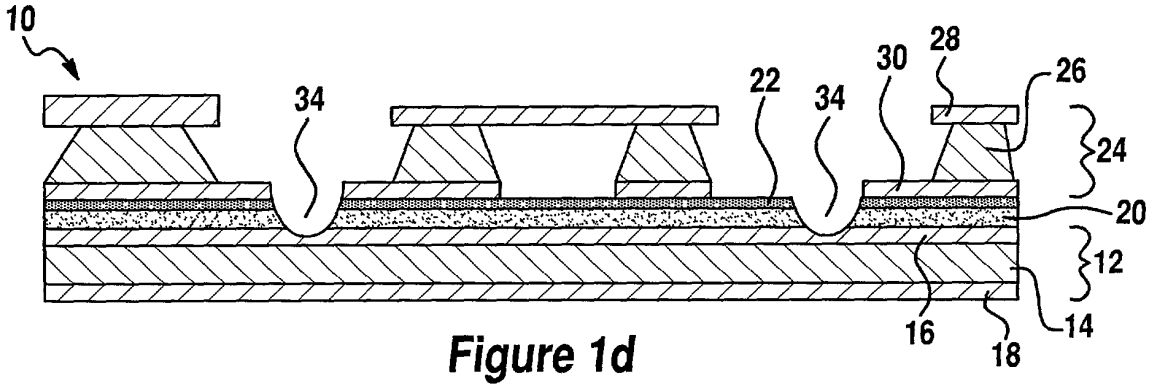


Figure 1d

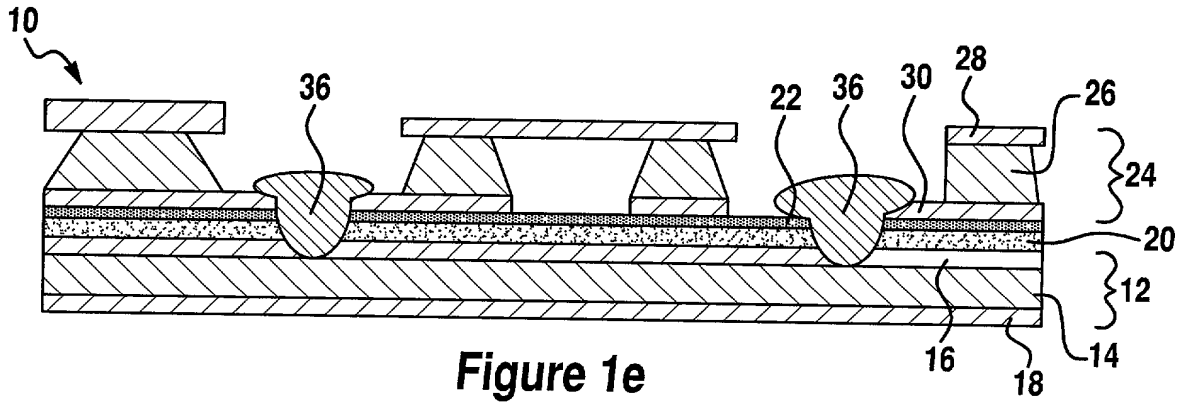


Figure 1e

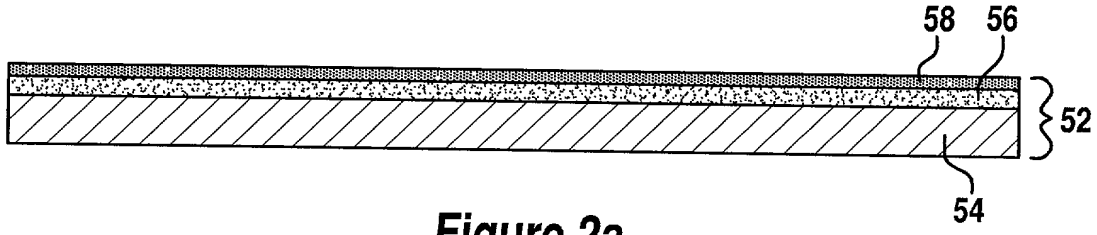


Figure 2a

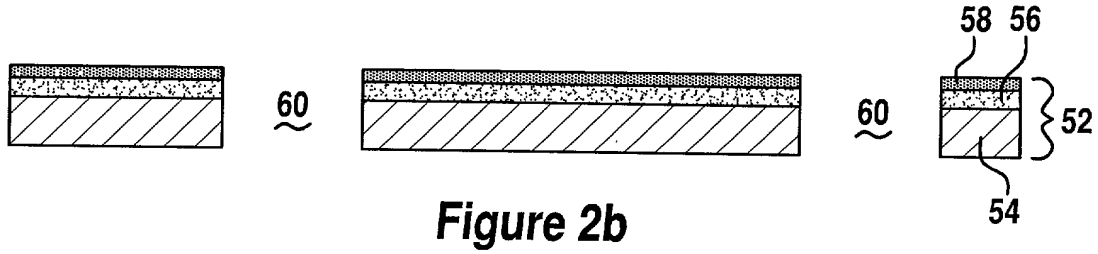


Figure 2b

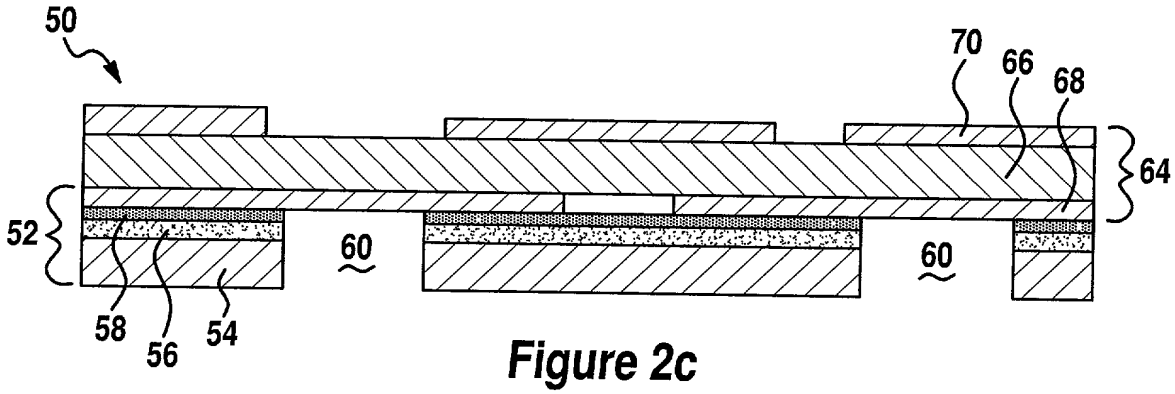


Figure 2c

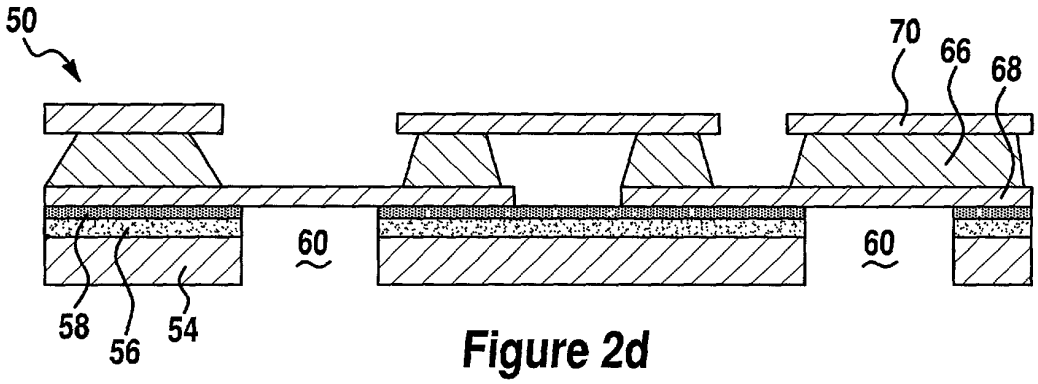


Figure 2d

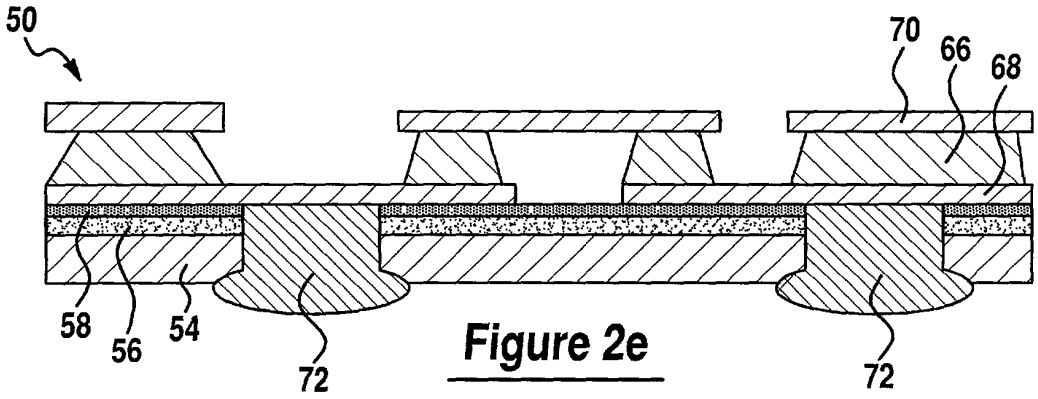


Figure 2e

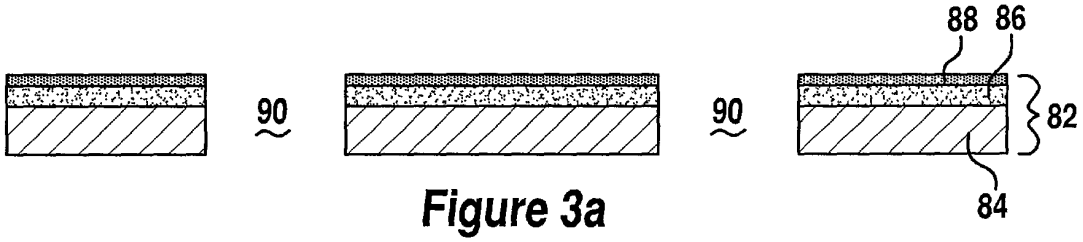


Figure 3a

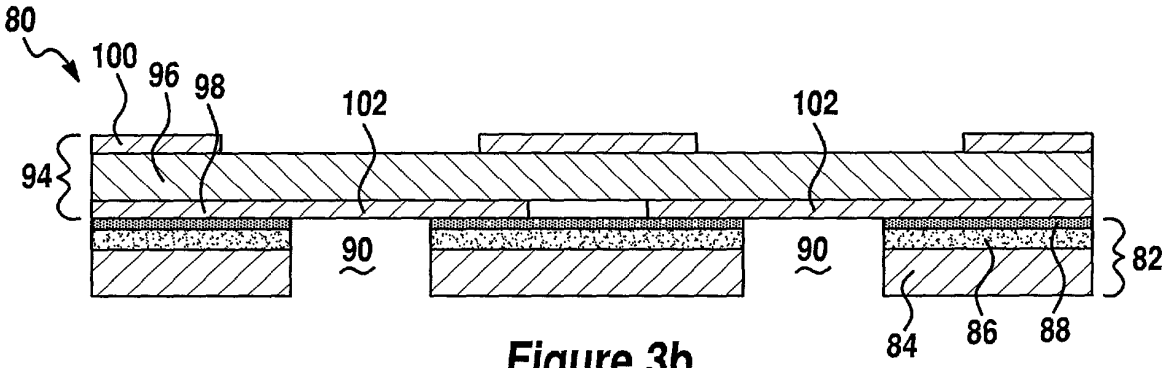


Figure 3b

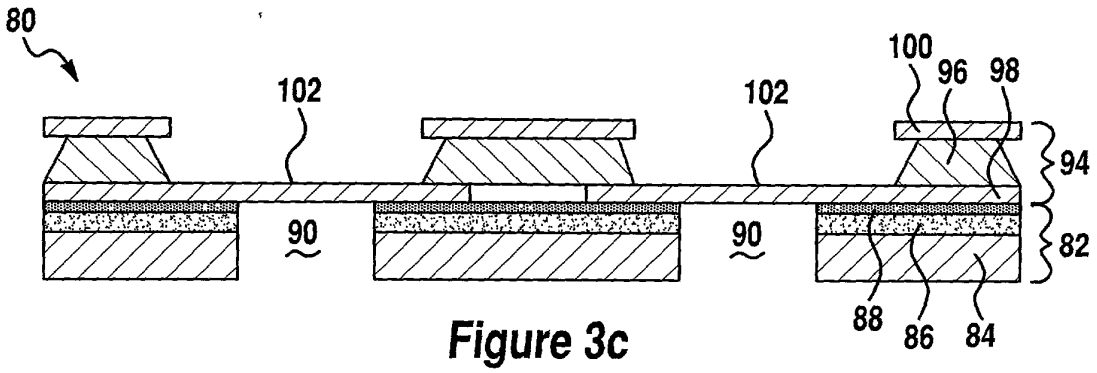


Figure 3c

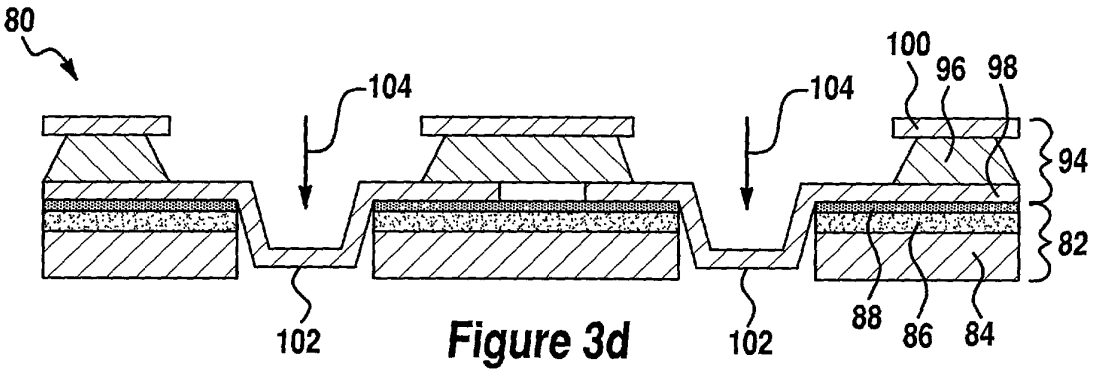


Figure 3d

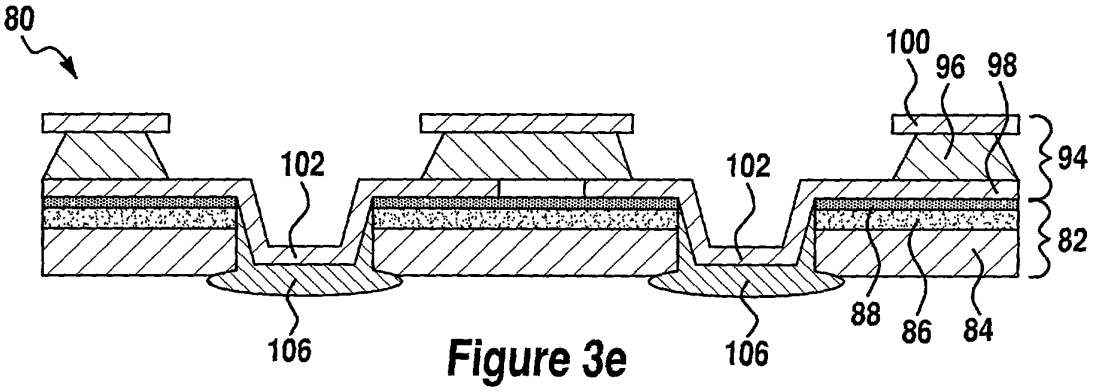


Figure 3e

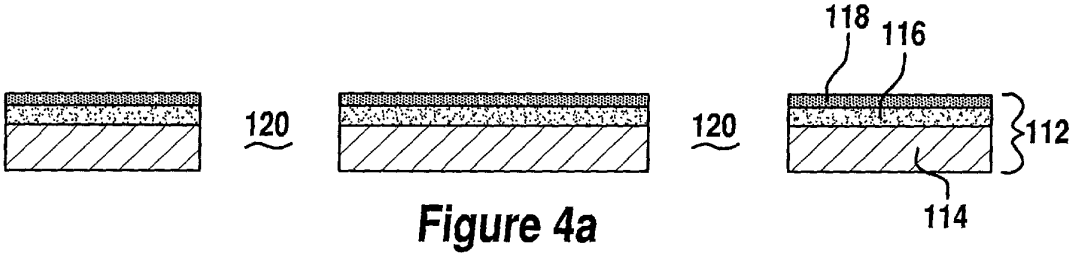


Figure 4a

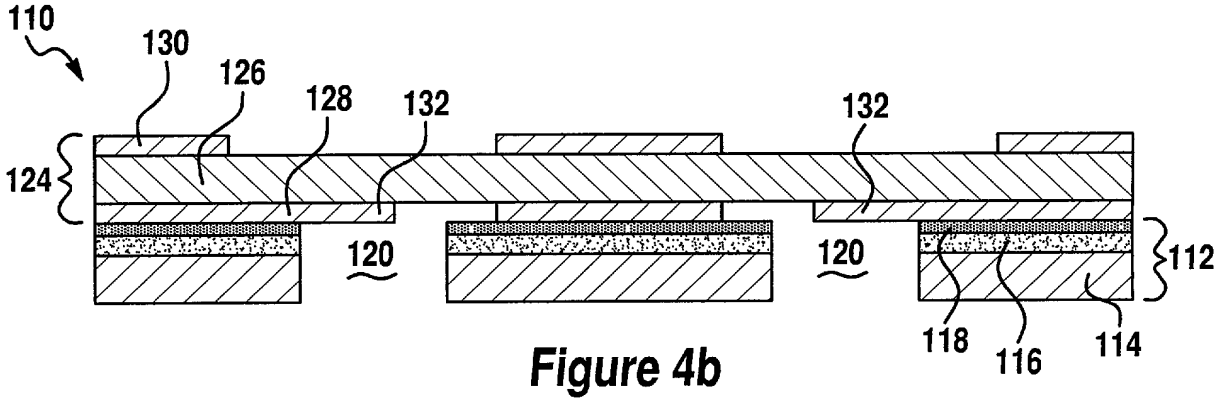


Figure 4b

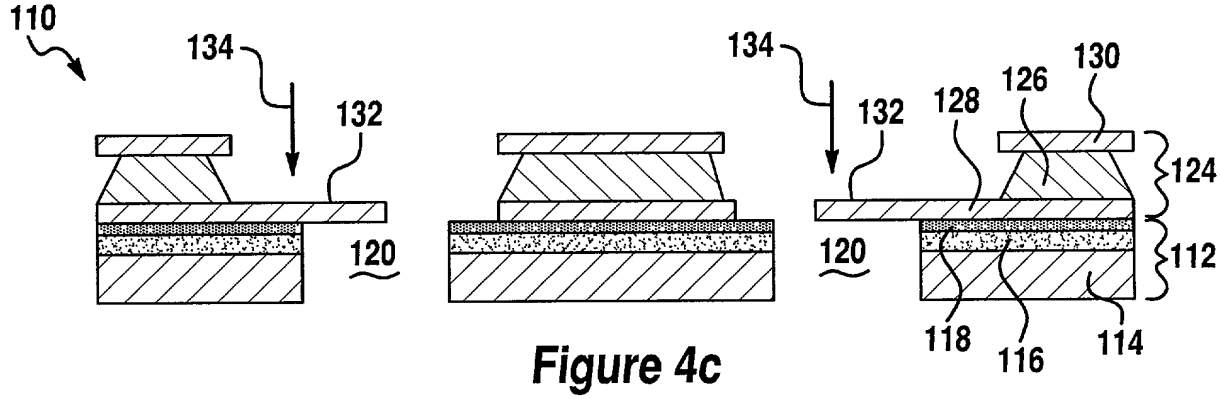


Figure 4c

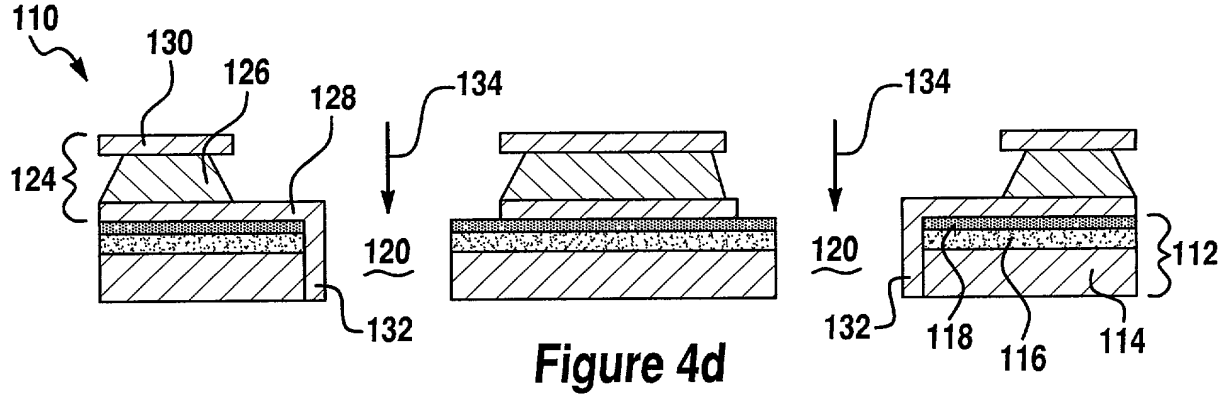


Figure 4d

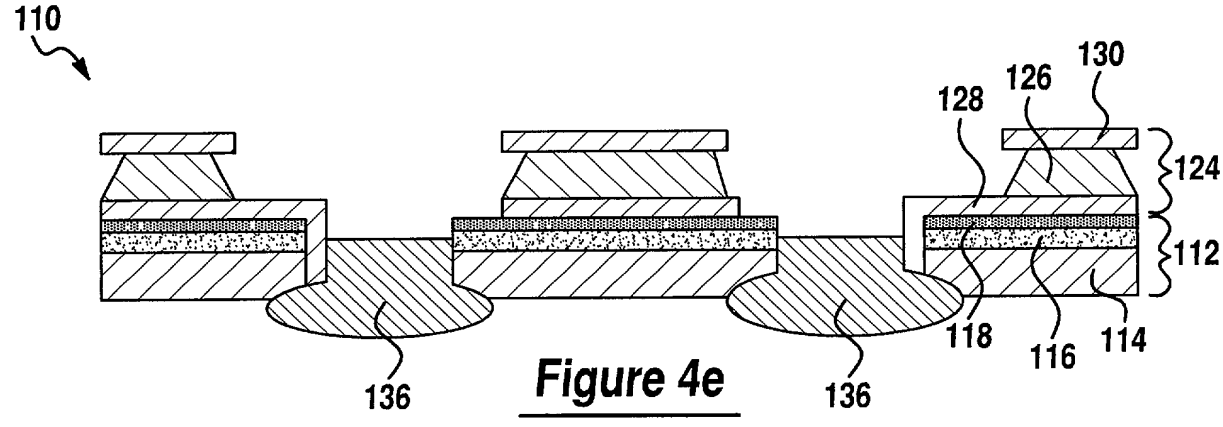


Figure 4e